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APPLICATION NO.	FILING DATE	FIRST NAMED INVENTOR	ATTORNEY DOCKET NO.	CONFIRMATION NO.
09/885,290	06/19/2001	Thomas Markson	55218-0519	3062

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SAN JOSE, CA 95110-1089

EXAMINER

TODD, GREGORY G

ART UNIT	PAPER NUMBER
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2157

MAIL DATE	DELIVERY MODE
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06/01/2007

PAPER

Please find below and/or attached an Office communication concerning this application or proceeding.

The time period for reply, if any, is set in the attached communication.

Office Action Summary

Application No.

09/885,290

Applicant(s)

MARKSON ET AL

Examiner

Gregory G. Todd

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-- The MAILING DATE of this communication appears on the cover sheet with the correspondence address --

Period for Reply

A SHORTENED STATUTORY PERIOD FOR REPLY IS SET TO EXPIRE 3 MONTH(S) OR THIRTY (30) DAYS, WHICHEVER IS LONGER, FROM THE MAILING DATE OF THIS COMMUNICATION.

- Extensions of time may be available under the provisions of 37 CFR 1.136(a). In no event, however, may a reply be timely filed after SIX (6) MONTHS from the mailing date of this communication.
- If NO period for reply is specified above, the maximum statutory period will apply and will expire SIX (6) MONTHS from the mailing date of this communication.
- Failure to reply within the set or extended period for reply will, by statute, cause the application to become ABANDONED (35 U.S.C. § 133). Any reply received by the Office later than three months after the mailing date of this communication, even if timely filed, may reduce any earned patent term adjustment. See 37 CFR 1.704(b).

Status

- 1) ☒ Responsive to communication(s) filed on 05 March 2007.
- 2a) ☐ This action is **FINAL**. 2b) ☒ This action is non-final.
- 3) ☐ Since this application is in condition for allowance except for formal matters, prosecution as to the merits is closed in accordance with the practice under *Ex parte Quayle*, 1935 C.D. 11, 453 O.G. 213.

Disposition of Claims

- 4) ☒ Claim(s) 1,2,7,8,10-12,15,40-43,45-47,49-53,55-57 and 59-68 is/are pending in the application.
- 4a) Of the above claim(s) _____ is/are withdrawn from consideration.
- 5) ☐ Claim(s) _____ is/are allowed.
- 6) ☒ Claim(s) 1,2,7,8,10-12,15,40-43,45-47,49-53,55-57 and 59-68 is/are rejected.
- 7) ☐ Claim(s) _____ is/are objected to.
- 8) ☐ Claim(s) _____ are subject to restriction and/or election requirement.

Application Papers

- 9) ☐ The specification is objected to by the Examiner.
- 10) ☐ The drawing(s) filed on _____ is/are: a) ☐ accepted or b) ☐ objected to by the Examiner.
Applicant may not request that any objection to the drawing(s) be held in abeyance. See 37 CFR 1.85(a).
Replacement drawing sheet(s) including the correction is required if the drawing(s) is objected to. See 37 CFR 1.121(d).
- 11) ☐ The oath or declaration is objected to by the Examiner. Note the attached Office Action or form PTO-152.

Priority under 35 U.S.C. § 119

- 12) ☐ Acknowledgment is made of a claim for foreign priority under 35 U.S.C. § 119(a)-(d) or (f).
- a) ☐ All b) ☐ Some * c) ☐ None of:
- ☐ Certified copies of the priority documents have been received.
 - ☐ Certified copies of the priority documents have been received in Application No. _____.
 - ☐ Copies of the certified copies of the priority documents have been received in this National Stage application from the International Bureau (PCT Rule 17.2(a)).

* See the attached detailed Office action for a list of the certified copies not received.

Attachment(s)

- | | |
|--|---|
| 1) <input checked="" type="checkbox"/> Notice of References Cited (PTO-892) | 4) <input type="checkbox"/> Interview Summary (PTO-413)
Paper No(s)/Mail Date. _____ |
| 2) <input type="checkbox"/> Notice of Draftsperson's Patent Drawing Review (PTO-948) | 5) <input type="checkbox"/> Notice of Informal Patent Application |
| 3) <input type="checkbox"/> Information Disclosure Statement(s) (PTO/SB/08)
Paper No(s)/Mail Date _____ | 6) <input type="checkbox"/> Other: _____ |

DETAILED ACTION

Response to Amendment

1. This office action is in response to applicant's amendment and request for continued examination filed, 05 March 2007, of application filed, with the above serial number, on 19 June 2001 in which claims 1-2, 7-8, 10-11, 15, 40-43, 45-46, 49-53, 55-56, and 59 have been amended, claims 3-6, 9, 13-14, 16-39, 44, 48, 54, and 58 have been cancelled, and claims 60-68 have been added. Claims 1-2, 7-8, 10-12, 15, 40-43, 45-47, 49-53, 55-57, and 59-68 are therefore pending in the application.

Specification

2. The specification is objected to as failing to provide proper antecedent basis for the claimed subject matter. See 37 CFR 1.75(d)(1) and MPEP § 608.01(o). Correction of the following is required: Applicant has amended claims 60, 63, and 66 to read "wherein the host processor does not *identify*" (emphasis added), however, Applicant refers to the specification for support wherein the specification specifically only defines wherein the host processor does not determine or know, and as Applicant has replaced "know" with "identify", is it reasonable that such a terminology change is significant and not supported.

Claim Rejections - 35 USC § 102

3. The following is a quotation of the appropriate paragraphs of 35 U.S.C. 102 that form the basis for the rejections under this section made in this Office action:

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A person shall be entitled to a patent unless –

(e) the invention was described in (1) an application for patent, published under section 122(b), by another filed in the United States before the invention by the applicant for patent or (2) a patent granted on an application for patent by another filed in the United States before the invention by the applicant for patent, except that an international application filed under the treaty defined in section 351(a) shall have the effects for purposes of this subsection of an application filed in the United States only if the international application designated the United States and was published under Article 21(2) of such treaty in the English language.

4. Claims 1-2, 7-8, 10, 15, 40-43, 45, 49-53, 55, and 59-68 are rejected under 35 U.S.C. 102(e) as being anticipated by Blumenau et al (hereinafter "Blumenau", 6,421,711).

As per Claim 1, Blumenau teaches a computer-implemented method of allocating storage to a host processor comprising:

a control processor receiving a request to allocate storage to the host processor (at least col. 31, lines 27-39; col. 33, lines 29-66; host requesting allocation of a volume); and

the control processor associating one or more logical units from among one or more storage units to the host processor by (at least col. 31, lines 9-51; col. 33 line 53 - col. 34 line 50; allocated and assigning LUN):

the control processor configuring a gateway device to map the one or more logical units to the host processor (at least col. 32 line 13 - col. 33 line 17; allocated and assigning LUN, the control processor being a part of the gateway device/gatekeeper and configuring itself);

the control processor configuring the one or more storage units to give the host processor access to the one or more logical units (at least col. 31, lines 9-51; col. 33 line 53 - col. 34 line 39; host or host controller having ability to access volumes);

wherein the host processor does not know which one or more logical units are associated with the host processor (at least col. 32, lines 13-43; host obtaining LUNs associated with it);

wherein the control processor is a different device than the gateway device, the host processor, and the one or more storage units (at least col. 42, lines 20-30; separate devices and interfaces); and

wherein the gateway device is a different device than the control processor, the host processor, and the one or more storage units (at least col. 42, lines 20-30; col. 31, lines 15-26; separate devices and interfaces; eg. gatekeeper being on a volume).

As per Claim 2. A method as recited in claim 1, wherein:

the control processor configuring the gateway device and the control processor configuring the one or more storage units are performed by the control processor without modification to an operating system of the host processor (at least col. 31, lines 9-51; col. 33 line 53 - col. 34 line 50);

the gateway device is included in a virtual storage layer (at least col. 32 line 13 - col. 33 line 17; storage subsystem volume / LUN);

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the host processor and the one or more storage units are included in a virtual server farm (at least col. 21 line 16 - col. 22 line 63; col. 7, lines 51-65; collection of servers);

the control processor is coupled through one or more storage networks to a plurality of storage gateways that includes the gateway device (at least col. 31, lines 9-51; col. 9, lines 18-43; Fig. 1-4; storage volumes); and

the plurality of storage gateways are coupled through the storage networks to the one ore more storage units (at least col. 31, lines 9-51; col. 9, lines 18-43; Fig. 1-4).

As per Claim 7. A method as recited in claim 1, further comprising:

the control processor causing the storage of first information that associates processors to logical units (at least col. 21 line 16 - col. 22 line 21; host to LUN to logical volume);

the control processor causing the storage of second information that associates logical units to storage units (at least col. 21 line 16 - col. 22 line 21; host to LUN to logical volume); and

the control processor associating the one or more logical units from among the one or more storage units to the host processor further comprises the control processor mapping the one or more logical units from among the one or more storage units to a boot port of the host processor by reconfiguring the gateway device to logically couple the one or more logical units to the boot port based on the stored first information and

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the stored second information (at least col. 32 line 13 - col. 33 line 17; boot from storage subsystem volume);

the control processor identifying one or more logical unit numbers corresponding to the one or more logical units (at least col. 32 line 13 - col. 34 line 59; col. 9, lines 44-57; col. 21, lines 16-55);

control processor instructing the gateway device to map the one or more logical unit numbers to the small computer system interface port zero of the host processor based on a unique processor identifier (at least col. 32 line 13 - col. 34 line 59; col. 9, lines 44-57); and

the control processor instructing the one or more storage units to give the host processor having the unique host identifier access to the one or more logical unit numbers (at least col. 31, lines 9-51).

As per Claim 8. A method as recited in claim 1, wherein the request to allocate storage to the host processor is a first request to allocate storage to the host processor, and the method further comprises:

based on the first request, the control processor generating a second request to allocate storage to the host processor (at least col. 11, lines 3-30; Fig. 1; col. 31, lines 9-61; col. 29 line 58 - col. 30 line 12);

wherein the control processor is communicatively coupled to a control database (at least col. 11, lines 3-30; Fig. 1; col. 31, lines 9-61; col. 29 line 58 - col. 30 line 12; gatekeeper with configuration database);

wherein the second request is directed from the control processor to a storage manager (at least col. 11, lines 3-30; Fig. 1; col. 31, lines 9-61; col. 29 line 58 - col. 30 line 12; gatekeeper with configuration database);

wherein the storage manager is communicatively coupled to the control processor, the control database, and a storage network that includes the gateway device (at least col. 11, lines 3-30; Fig. 1; col. 31, lines 9-61; col. 29 line 58 - col. 30 line 12; gatekeeper with configuration database); and

the method further comprises the control processor causing the storage manager to issue instructions to the one or more storage units to give the host processor access to the one or more logical units (at least col. 31, lines 9-51)

As per Claim 10. A method as recited in claim 1, wherein the request to allocate storage specifies a first amount of storage (eg. a single logical volume; see col. 1, lines 40-58) , and wherein the control processor associating the one or more logical units further comprises:

the control processor identifying the one or more logical units of the one or more storage units that, when combined, have a second amount of storage that is at least as great as the first amount of storage specified in the request (at least col. 32 line 13 - col. 34 line 59; col. 9, lines 44-57).

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As per Claim 15. A method as recited in claim 1, wherein:

the one or more logical units associated with the host processor include at least a first logical unit from a first volume of a first storage unit of the one or more storage units and at least a second logical unit from a second volume of a second storage unit of the one or more storage units (at least Fig. 19; col. 21, lines 16-67);

the request to allocate storage specifies a parameter selected from the group consisting of an amount of storage to be allocated and a type of storage to be allocated (at least col. 31 line 9 - col. 32 line 12; col. 6 line 64 - col. 7 line 65; col. 9, lines 44-57; col. 32, lines 58-67; col. 34, lines 2-17).

the control processor is separate from the gateway device, the host processor, and the one or more storage units (at least col. 31, lines 9-51; col. 9, lines 18-43; Fig. 1-4); and

the gateway device is separate from the control processor, the host processor, and the one or more storage units (at least col. 31, lines 9-51; col. 9, lines 18-43; Fig. 1-4).

As per Claim 60. A method as recited in Claim 1, wherein the host processor does not identify which one or more logical units are associated with the host processor (at least col. 11 line 57 – col. 12 line 31; restrict volumes seen ("known") by any one host).

As per Claim 61. A method as recited in Claim 1, wherein:

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the one or more logical units are associated with one or more logical unit numbers (at least col. 32 line 13 - col. 34 line 59; col. 9, lines 44-57; col. 21, lines 16-55); and

the host processor does not know the one or more logical unit numbers for the one or more logical units that are associated with the host processor (at least col. 11 line 57 – col. 12 line 31; restrict volumes seen by any one host).

As per Claim 62. A method as recited in Claim 1, wherein:

the host processor is a first host processor (at least Fig. 1-3);

the one or more logical units include a first logical unit and a second logical unit (at least Fig. 1-3);

the one or more storage units include a first storage unit and a second storage unit (at least Fig. 1-3);

the first logical unit is associated with the first storage unit (at least Fig. 1-3);

the second logical unit is associated with the second storage unit (at least Fig. 1-3);

the control processor associates the first logical unit and the second logical unit to the first host processor at a first time (at least col. 31, lines 9-51; col. 33 line 53 - col. 34 line 50; allocated and assigning LUN); and

the method further comprises:

at a second time that is after the first time, the control processor associating the second logical unit with a second host processor by:

the control processor configuring the gateway device to map the second logical unit to the second host processor instead of the first host processor (at least col. 32 line 13 - col. 33 line 17; allocated and assigning LUN, the control processor being a part of the gateway device/gatekeeper and configuring itself);

the control processor configuring the second storage unit to give the second host processor access to the second logical unit instead of the first host processor (at least col. 31, lines 9-51; col. 33 line 53 - col. 34 line 39; host or host controller having ability to access volumes);

wherein the second host processor does not determine that the second logical unit is associated with the second host processor (at least col. 32, lines 13-43; host obtaining LUNs associated with it);

wherein the first logical unit remains associated with the first host processor (at least Fig. 1-3);

at a third time that is after the second time, the control processor associating the second logical unit with the first host processor by:

the control processor configuring the gateway device to map the second logical unit to the first host processor instead of the second host processor (at least col. 32 line 13 - col. 33 line 17; allocated and assigning LUN, the control processor being a part of the gateway device/gatekeeper and configuring itself);

the control processor configuring the second storage unit to give the first host processor access to the second logical unit instead of the second host processor (at

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least col. 31, lines 9-51; col. 33 line 53 - col. 34 line 39; host or host controller having ability to access volumes);

wherein the first host processor does not determine that the second logical unit is associated with the first host processor (at least col. 32, lines 13-43; host obtaining LUNs associated with it); and

wherein the first logical unit remains associated with the first host processor (at least Fig. 1-3).

Claims 40-43, 45, 49-53, 55, 59, and 63-68 do not substantially add or define any additional limitations over claims 1, 2, 7-8, 10, 15, and 60-62 and therefore are rejected for similar reasons.

Claim Rejections - 35 USC § 103

5. The following is a quotation of 35 U.S.C. 103(a) which forms the basis for all obviousness rejections set forth in this Office action:

(a) A patent may not be obtained though the invention is not identically disclosed or described as set forth in section 102 of this title, if the differences between the subject matter sought to be patented and the prior art are such that the subject matter as a whole would have been obvious at the time the invention was made to a person having ordinary skill in the art to which said subject matter pertains. Patentability shall not be negated by the manner in which the invention was made.

6. Claims 11-12, 46-47, and 56-57 are rejected under 35 U.S.C. 103(a) as being unpatentable over Blumenau in view of Ofer et al (hereinafter "Ofer", 6,260,109).

As per Claim 11. A method as recited in claim 1, wherein the request is a first request, and the control processor associating the one or more logical units further comprises:

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the control processor issuing a second request to allocate one or more volumes on one of the one or more storage units (at least col. 31, lines 27-39; col. 33 line 29 - col. 34 line 50);

the control processor causing the volume to be configured for use with the host processor (at least col. 31, lines 9-51);

the control processor issuing first instructions to the one or more storage units to bind the host processor to the volume by giving the host processor access to the volume (at least col. 33 line 29 - col. 34 line 50);

the control processor issuing second instructions to the gateway device to bind the volume to the host processor (at least col. 33 line 29 - col. 34 line 50; eg. gatekeeper).

Blumenau fails to explicitly teach the volume being concatenated. However, the use and advantages for using such concatenation is well known to one skilled in the art at the time the invention was made as evidenced by the teachings of Ofer (at least Abstract). Therefore, it would have been obvious to one of ordinary skill in the art at the time the invention was made to incorporate Ofer's use of concatenation into Blumenau's system as this would enhance Blumenau's RAID arrays and subsequently allocated logical volumes to be combined together as this is well known in the art in expanding storage.

As per Claim 12. A method as recited in claim 11, further comprising:

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the control processor determining that the second instructions have failed to bind the concatenated volume to the host processor (at least col. 33 line 29 - col. 34 line 50);

the control processor issuing third instructions to the one or more storage units to un-bind the host processor from the concatenated volume (at least col. 33 line 29 - col. 34 line 50; removing and deallocating);

the control processor determining that the first instructions have failed to bind the host processor to the volume (at least col. 33 line 29 - col. 34 line 50); and

the control processor issuing fourth instructions to the one or more storage units to break the volume (at least col. 33 line 29 - col. 34 line 50).

Claims 46, 47 and 56-57 do not substantially add or define any additional limitations over claims 11-12 and therefore are rejected for similar reasons.

Response to Arguments

7. Applicant's arguments filed 05 March 2007 have been fully considered but they are not persuasive.

Applicant argues, in substance, that Blumenau does not teach the amended features of claim 1, including wherein the host processor does not know which one or more logical units are associated with the host processor;

wherein the control processor is a different device than the gateway device, the host processor, and the one or more storage units; and

wherein the gateway device is a different device than the control processor, the host processor, and the one or more storage units.

However, Blumenau teaches the features of the claims as amended, as Blumenau teaches wherein the host processor does not know which one or more logical units are associated with the host processor (at least col. 32, lines 13-43; host obtaining LUNs associated with it). While Applicant relies on the claim language where Blumenau states “the host must be programmed to seek out the LUNs that it can access”, this statement, on the contrary, clearly states that the host must **seek out** the LUNs, thus, there would be no need to seek out the LUNs if the LUNs were known prior; so, while the host eventually knows the LUNs, they are not known, as they must be sought after in the first place. Further, the mere reference to seeking out the LUNs does not necessitate knowing the LUNs, rather, the seeking step could be taken to gather any and all LUNs it can access and not knowing which LUNs are thereby associated with what. Also, the terminology of *knowing* something is narrow enough, along with the negative limitation, so as to *not* “know” one or more LUNs, would encompass having sought out *some* LUNs associated with the host processor, but not *all* LUNs associated with that host processor, in addition to how well the host processor must *know* the LUNs. Thus, in the case of the negative limitation terminology, Blumenau teaches the claims as amended.

Regarding wherein the control processor is a different device than the gateway device, the host processor, and the one or more storage units; and

wherein the gateway device is a different device than the control processor, the host processor, and the one or more storage units. Blumenau teaches that all entities be separate, along with the gatekeeper being on a volume LUN0 (at least col. 42, lines 20-30; col. 31, lines 15-26; col. 34, lines 40-59). Also, the gatekeeper facility is termed separately from the controller and host, and Blumenau even mentions the controller being replaced, and the system being restored afterward. Thus, while the system might include the gatekeeper facility along with the controller and hosts, each is a separate device with a separate function. Just as in the current invention, for example, a control processor cannot act alone, and while it is a separate device, per se, the control processor interacts with other devices, and the broad definition of a device along with the definition of a processor, encompasses a physical processor by itself, or could represent different processing functions on a physical processor while being separate devices.

In response to applicant's argument that Blumenau's gatekeeper and controller are not separate devices, a recitation of the intended use of the claimed invention must result in a structural difference between the claimed invention and the prior art in order to patentably distinguish the claimed invention from the prior art. If the prior art structure is capable of performing the intended use, then it meets the claim. In this case, as Blumenau refers to the devices separately, and the mere use of different terminology infers more than a single device and being different. Assuming the devices were somehow the 'same', there are no structural differences as they are each capable of performing the intended use.

Conclusion


8. The prior art made of record and not relied upon is considered pertinent to applicant's disclosure. Newly cited Aziz, in addition to previously cited Pothapragada et al, Sheets et al, Blickenstaff et al, Aziz et al, Denning et al, Nguyen et al, Nolan et al ('526, '278), Popelka et al, Hickman et al, Tamer et al, and Blumenau '442 are cited for disclosing pertinent information related to the claimed invention. Applicants are requested to consider the prior art reference for relevant teachings when responding to this office action.

9. Any inquiry concerning this communication or earlier communications from the examiner should be directed to Gregory G. Todd whose telephone number is (571)272-4011. The examiner can normally be reached on Monday - Friday 9:00am-6:00pm w/ first Fridays off.

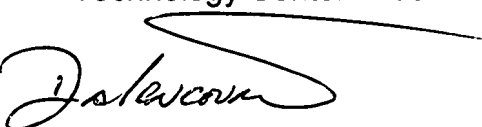
If attempts to reach the examiner by telephone are unsuccessful, the examiner's supervisor, Ario Etienne can be reached on (571)272-4001. The fax phone number for the organization where this application or proceeding is assigned is 703-872-9306.

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Information regarding the status of an application may be obtained from the Patent Application Information Retrieval (PAIR) system. Status information for published applications may be obtained from either Private PAIR or Public PAIR. Status information for unpublished applications is available through Private PAIR only. For more information about the PAIR system, see <http://pair-direct.uspto.gov>. Should you have questions on access to the Private PAIR system, contact the Electronic Business Center (EBC) at 866-217-9197 (toll-free).

Gregory Todd 
Patent Examiner

Technology Center 2100


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